In the Claims:

1. (canceled)

2. (new) A process of initializing the state of an output memory circuit of a scan cell located at the boundary of a logic circuit within an integrated circuit having a logic circuit comprising:

A. scanning data into an input memory circuit of the cell while maintaining the cell in a first mode providing normal operation of the logic circuit;

B. placing the cell in a second mode that disables normal operation of the logic circuit; and

C. transferring the data scanned into the input memory circuit into the output memory circuit simultaneous with the placing the cell in a mode that disables normal operation of the logic circuit.

3. (new) The process of claim 2 in which the first mode is a preload scan operation and the second mode is a test operation.

4. (new) The process of claim 2 in which the first memory circuit is a capture/shift memory circuit.

5. (new) The process of claim 2 in which the second memory circuit is a latchable buffer circuit.

6. (new) The process of claim 2 in which the maintaining includes enabling a first transmission gate between the logic circuit and the output memory circuit and disabling a second transmission gate between the input memory circuit and the output memory circuit.

7. (new) The process of claim 2 in which the placing includes disabling a first transmission gate between the

logic circuit and the output memory circuit and enabling a second transmission gate between the input memory circuit and the output memory circuit.